VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A [apparatus] transistor device, comprising:

a substrate having a source region, a drain region[,] and a channel region [having], in which at least one of the source, drain and channel regions has a void to [provide a barrier to lines of force to reduce leakage current] place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress; and

a gate region formed over the channel region.

2. (Amended) The [apparatus] transistor of claim 1 wherein [said] the void is located substantially in a center of [said] the channel region.

3. (Amended) The [apparatus] transistor of claim 1 wherein [said] the void is approximately 50 nm across.

4. (Amended) The [apparatus] transistor of claim 1 wherein [said] the void is located at a depth of approximately 1000 angstroms in [said] the channel region.

5. (Canceled)

6. (Amended) The [apparatus] transistor of claim [5] 1 wherein [said] the void is located in the channel region and near an edge of [said] the channel region adjacent to [said] the source region.

7. (Amended) The [apparatus of 6 further comprising a] transistor of claim 1 wherein the void is located in the channel region near an edge of the channel region adjacent to the drain region.

8. (Amended) A[n apparatus] transistor, comprising:

[a gate region; and]

a substrate having a source region[,] and a drain region, a channel region, [and] in which [and] a void is located below [said] the source region to [provide a

barrier to lines of force to reduce leakage current] place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress; and

a gate region above the channel region.

9. (Amended) The [apparatus] transistor of claim 8 wherein a void is also located below [said] the drain region.

10. (Amended) The [apparatus] transistor of claim 9 wherein [said] the source and drain regions [and said drain regions] are under compressive stress.

11. (Amended) The [apparatus] transistor of claim 8 wherein [said] the source region is under tensile stress.

12. (Amended) The [apparatus] transistor of claim 8 wherein [said] the drain region is under compressive stress.

13. (Amended) The [apparatus] transistor of claim 8 wherein [said] the gate region is polysilicon.

14. (Amended) The [apparatus] transistor of claim 8 wherein [said] the gate region is metal.

15. (Amended) A[n apparatus] transistor comprising:

[a gate region having a void to provide a barrier to lines of force to reduce leakage current; and]

a substrate having a source region, a drain region[,] and a channel region; and

a gate region having a void to place the substrate under mechanical stress to alter carrier mobility due to the stress.

16. (Canceled)

17. (Amended) The [apparatus] transistor of claim 15 wherein [said] the gate region is polysilicon.

18. (Amended) The [apparatus] transistor of claim 15 wherein [said] the gate region is metal.